THAT WHICH IS CLAIMED IS:

1. A logic circuit for performing a logic function, and having N data inputs and M data outputs, N being at least equal to 2 and M being at least equal to 1, the logic circuit comprising:

at least one logic gate for performing the logic function in at least two different ways, the way in which the logic function is performed being based upon a value of a function selection signal such that for identical data received at the N data inputs and for different values of the function selection signal, at least one of polarities of certain internal nodes of the logic circuit are not identical and current consumption of the logic circuit is not identical.

2. A logic circuit according to Claim 1, wherein said at least one logic gate has N inputs linked to the N data inputs of the logic circuit, and M outputs linked to the M data outputs of the logic circuit, said at least one logic gate for performing first and second logic functions based upon the value of the function selection signal; and further comprising:

reversing means for reversing the data applied to the N inputs of said at least one logic gate, and for reversing the data delivered by said at least one logic gate based upon the value of the function selection signal.

3. A logic circuit according to Claim 2, wherein said reversing means comprises a plurality of

EXCLUSIVE-OR gates, each EXCLUSIVE-OR gate having an input for receiving the function selection signal.

4. A logic circuit according to Claim 1, wherein said at least one logic gate comprises a plurality of logic gates for performing a NAND logic function when the function selection signal has a first logic value, and for performing a NOR logic function when the function selection signal has a second logic value.

5. A logic circuit according to Claim 1, wherein the function selection signal is randomly generated.

6. A logic circuit according to Claim 1, wherein said at least one logic gate comprises:

a first group of transistors for performing a first logic function;

a second group of transistors for performing a second logic function; and

function selection means connected to said first and second groups of transistors and having an input for receiving the function selection signal for validating one of the first and second logic functions at the output of said at least one logic gate based upon the value of the function selection signal.

7. A logic circuit according to Claim 6, wherein said first group of transistors comprises first and second stages of transistors, and said second group of transistors comprises first and second stages of transistors; and wherein said function selection means

comprises at least one first selection transistor for short-circuiting the first stages of transistors based upon the value of the function selection signal.

8. A logic circuit according to Claim 7, wherein said function selection means further comprises at least one second selection transistor for interrupting conductive paths in the second stages of transistors based upon the value of the function selection signal.

9. A logic circuit according to Claim 6, wherein the first logic function is a NAND logic function and the second logic function is a NOR logic function.

10. A logic circuit according to Claim 1, wherein the logic function is an encryption function.

11. A secured integrated circuit device comprising:

an encryption circuit comprising

a plurality of encryption blocks, each encryption block for performing a logic function in at least two different ways, the way in which the logic function is performed being based upon a value of a function selection signal such that for identical data received and for different values of the function selection signal, at least one of polarities of certain internal nodes of said encryption circuit are not identical and

current consumption of said encryption circuit is not identical; and

a random signal generator connected to said plurality of encryption blocks for randomly providing the function selection signal to each encryption block.

12. A secured integrated circuit device according to Claim 11, wherein the value of the function selection signal is randomly modified at least after each reset of the secured integrated circuit device.

13. A secured integrated circuit device according to Claim 11, wherein said random signal generator provides a respective function selection signal to each encryption block, with the value of each respective function selection signal being independent of the value of the function selection signals applied to other encryption blocks.

14. A secured integrated circuit device according to Claim 11, wherein each encryption block performs first and second logic functions based upon the value of the function selection signal; said encryption circuit further comprising:

reversing circuitry for reversing data applied to inputs of each encryption block, and for reversing data delivered each encryption block based upon the value of the function selection signal.

15. A secured integrated circuit device according to Claim 14, wherein said reversing circuitry comprises a plurality of EXCLUSIVE-OR gates, each

EXCLUSIVE-OR gate having an input for receiving the function selection signal.

16. A secured integrated circuit device according to Claim 11, wherein each encryption block comprises a plurality of logic gates for performing a NAND logic function when the function selection signal has a first logic value, and for performing a NOR logic function when the function selection signal has a second logic value.

17. A secured integrated circuit device according to Claim 11, wherein each encryption block comprises:

a first group of transistors for performing a first logic function;

a second group of transistors for performing a second logic function; and

a function selection circuit connected to said first and second groups of transistors and having an input for receiving the function selection signal for validating one of the first and second logic functions at an output of said encryption block based upon the value of the function selection signal.

18. A secured integrated circuit device according to Claim 17, wherein said first group of transistors comprises first and second stages of transistors, and said second group of transistors comprises first and second stages of transistors; and wherein said function selection circuit comprises at least one first selection transistor for short-

circuiting the first stages of transistors based upon the value of the function selection signal.

19. A secured integrated circuit device according to Claim 18, wherein said function selection circuit further comprises at least one second selection transistor for interrupting conductive paths in the second stages of transistors based upon the value of the function selection signal.

20. A secured integrated circuit device according to Claim 17, wherein the first logic function is a NAND logic function and the second logic function is a NOR logic function.

21. A secured integrated circuit device according to Claim 11, further comprising a central processing unit (CPU) connected to said encryption circuit.

22. A secured integrated circuit device according to Claim 17, wherein said encryption circuit and said random signal generator are configured so that the secured integrated circuit device is at least one of a smart card or another type of portable electronic object.

23. A method for scrambling operation of a logic circuit that performs a logic function, the logic circuit having N data inputs and M data outputs, with N being at least equal to 2 and M being at least equal to 1, the method comprising:

performing the logic function in at least two different ways using at least one logic gate, the way

the logic function is performed being determined by a value of a function selection signal such that for identical data received at the N data inputs and for different values of the function selection signal, at least one of polarities of certain internal nodes of the logic circuit are not identical and current consumption of the logic circuit is not identical; and

refreshing the function selection signal at predetermined instants so that operation of the logic circuit is scrambled.

24. A method according to Claim 23, wherein the function selection signal is randomly applied to the at least one logic gate.

25. A method according to Claim 23, wherein the at least one logic gate has N inputs linked to the N data inputs of the logic circuit, and M outputs linked to the M data outputs of the logic circuit, the at least one logic gate for performing first and second logic functions based upon the value of the function selection signal, and further comprising:

reversing the data applied to the N inputs of the at least one logic gate based upon the value of the function selection signal; and

reversing the data delivered by the at least one logic gate based upon the value of the function selection signal.

26. A method according to Claim 25, wherein the reversing is performed using a reversing circuit comprising a plurality of EXCLUSIVE-OR gates, each

EXCLUSIVE-OR gate having an input for receiving the function selection signal.

27. A method according to Claim 23, wherein the at least one logic gate comprises a plurality of logic gates for performing a NAND logic function when the function selection signal has a first logic value, and for performing a NOR logic function when the function selection signal has a second logic value.

28. A method according to Claim 23, wherein the at least one logic gate comprises a first group of transistors for performing a first logic function, and a second group of transistors for performing a second logic function, and further comprising:

using a function selection circuit connected to the first and second groups of transistors and having an input for receiving the function selection signal for validating one of the first and second logic functions at the output of the at least one logic gate based upon the value of the function selection signal.

29. A method according to Claim 28, wherein the first group of transistors comprises first and second stages of transistors, and the second group of transistors comprises first and second stages of transistors; and wherein the function selection circuit comprises at least one first selection transistor for short-circuiting the first stages of transistors based upon the value of the function selection signal.

30. A method according to Claim 29, wherein the function selection circuit further comprises at

least one second selection transistor for interrupting conductive paths in the second stages of transistors based upon the value of the function selection signal.

31. A method according to Claim 27, wherein the first logic function is a NAND logic function and the second logic function is a NOR logic function.

32. A method according to Claim 23, wherein the logic function is an encryption function.